46. (New) A state engine as claimed in claim 32, further comprising:

a plurality of state engines, wherein one or more of said state engines are applied to a system bus and wherein said one or more of said state engines operate separately from each other.

41. (New) A state engine as claimed in claim 19, wherein said memory is within said state element.

42. (New) A state engine as claimed in claim 19, wherein said state engine includes a plurality of state elements which comprise a plurality of local shared memories which provides a composite bandwidth that is a sum of all bandwidths associated with each one of said plurality of local shared memories.

43. (New) A state engine as claimed in claim 42, wherein state transactions are processed with said state engine and accesses to shared memory are passed on a system bus.

44. (New) A state engine as claimed in claim 42, wherein each of said plurality of state elements includes a single serialization access point resulting in a plurality of serialization access points within said state engine.

45. (New) A state engine as claimed in claim 42, wherein said plurality of state elements perform as a plurality of partitioned processing functions.

a memory connected to said at least one state element means and configured to store said shared state.

37. (Previously Presented) A parallel processor as claimed in claim 32, implemented on a single silicon chip.

38. (Previously Presented) A state engine receiving multiple requests from a parallel processor for a shared state, the state engine comprising:

means for operating, atomically, on said shared state in response to a request made by said parallel processor, wherein

said request includes at least a command directing said means for operating on how to perform an operation on said shared state;

a memory connected to said means for operating and configured to store said shared state; and

means to supply data to update said shared state.

39. (New) A state engine as claimed in claim 19, wherein said operation results in a change of said shared state.

40. (New) A state engine as claimed in claim 19, wherein said state engine is a programmable entity capable of executing shared memory instructions.

35. (Previously Presented) A computer system comprising a parallel processor, said parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state, the state engine comprising:

at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor, wherein

said request includes at least a command directing said at least one state element means on how to perform an operation on said shared state; and

a memory connected to said at least one state element means and configured to store said shared state.

36. (Previously Presented) A network processor comprising a parallel processor, said parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state, the state engine comprising:

at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor, wherein

said request includes at least a command directing said at least one state element means on how to perform an operation on said shared state; and

arithmetic unit adapted to perform the operation on said state in said local memory, and command and control logic to control said operation.

32. (Previously Presented) A parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state, the state engine comprising:

at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor, wherein

said request includes at least a command directing said at least one state element means on how to perform an operation on said shared state; and

a memory connected to said at least one state element means and configured to store said shared state.

33. (Previously Presented) A parallel processor as claimed in claim 32, wherein said parallel processor is an array processor.

34. (Previously Presented) A parallel processor as claimed in claim 33, wherein said array processor is a SIMD processor.

27. (Previously Presented) A state engine as claimed in claim 19, further comprising a plurality of said state element means organized into state cell means, whereby operations performed on said shared state are pipelined.

28. (Previously Presented) A state engine as claimed in claim 27, further comprising a plurality of said state cell means, whereby to allow multiple requests to be handled concurrently.

29. (Previously Presented) A state engine as claimed in claim 28, further comprising input and output interconnect means providing access to and from said state cell means, a bus interface for said input and output interconnect means, said bus interface interfacing with a system bus and a control unit of a processing element for controlling accesses to said shared state.

30. (Previously Presented) A state engine as claimed in claim 27, wherein each said state element means comprises local memory, and each field of a data record is stored in a respective memory of a respective state element means.

31. (Previously Presented) A state engine as claimed in claim 19, wherein each said state element means comprises a local memory for said shared state, an

21. (Previously Presented) A state engine as claimed in claim 19, wherein said shared state comprises a single item of state.

22. (Previously Presented) A state engine as claimed in claim 19, wherein said shared state comprises multiple items of state.

23. (Previously Presented) A state engine as claimed in claim 19, wherein said state comprises a single storage location or a data structure in storage.

24. (Previously Presented) A state engine as claimed in claim 19, wherein the operation performed by said at least one state element means is carried out as a fixed or hardwired operation.

25. (Previously Presented) A state engine as claimed in claim 24, further comprising means to supply data to update said shared state.

26. (Previously Presented) A state engine as claimed in claim 24, further comprising means for sending a command and data to said shared state, whereby said operation is programmable.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-18 (canceled)

19. (Previously Presented) A state engine receiving multiple requests from a parallel processor for a shared state, the state engine comprising:

at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor, wherein

said request includes at least a command directing said at least one state element means on how to perform an operation on said shared state; and

a memory connected to said at least one state element means and configured to store said shared state.

20. (Previously Presented) A state engine as claimed in claim 19, wherein the operation performed by said at least one state element means is a single read-modify-write operation.

Patent
Attorney's Docket No. 0120-034

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Anthony SPENCER	)	Confirmation No.: 5040
	)	
Application No.: 10/534,430	)	Group Art Unit: 2185
	)	
Filed: July 18, 2005	)	Examiner: Yong J. Choe
	)	
For: STATE ENGINE FOR DATA PROCESSOR	)	
	)	

AMENDMENT UNDER 37 C.F.R.§1.111

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

In complete response to the Office Action dated October 30, 2008, kindly amend the above-identified application as follows: